

FIG. 1A

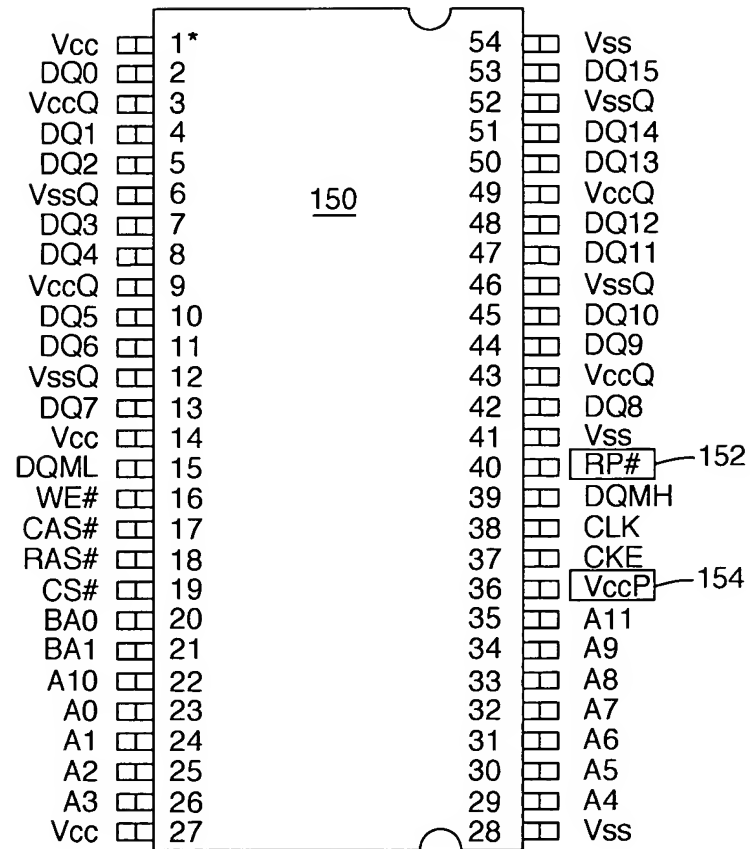


FIG. 1B

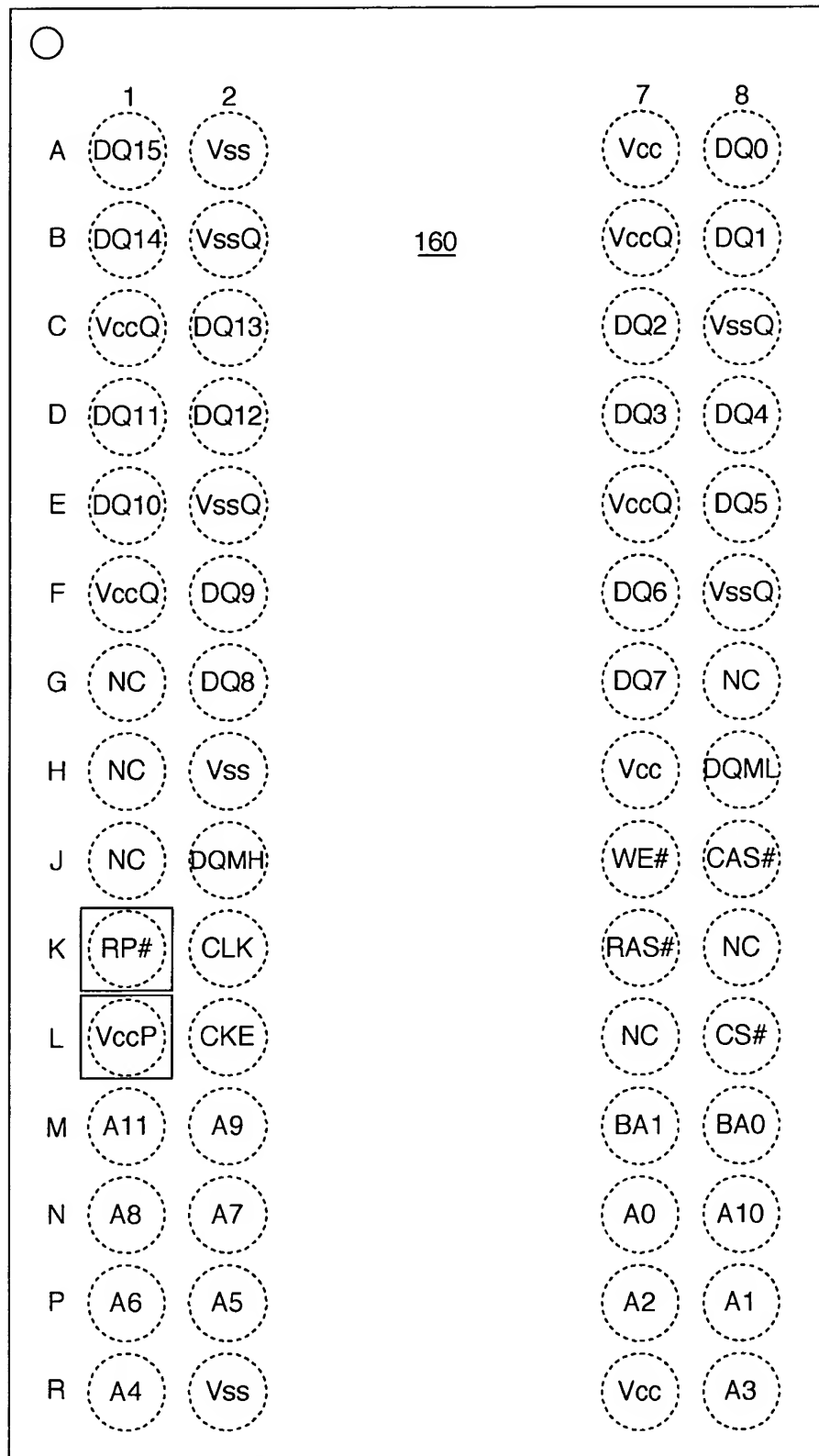


FIG. 1C

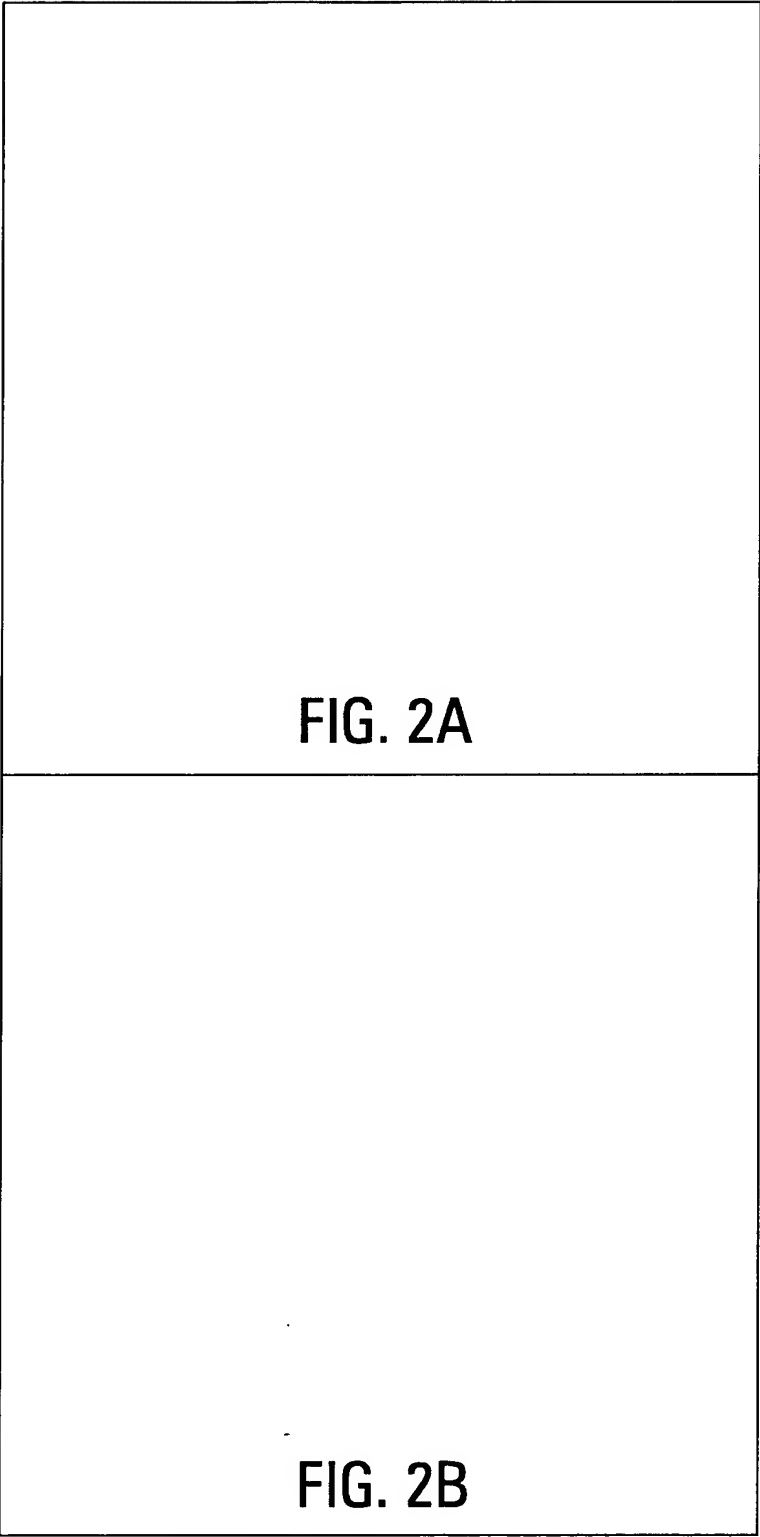


FIG. 2A

FIG. 2B

FIG. 2

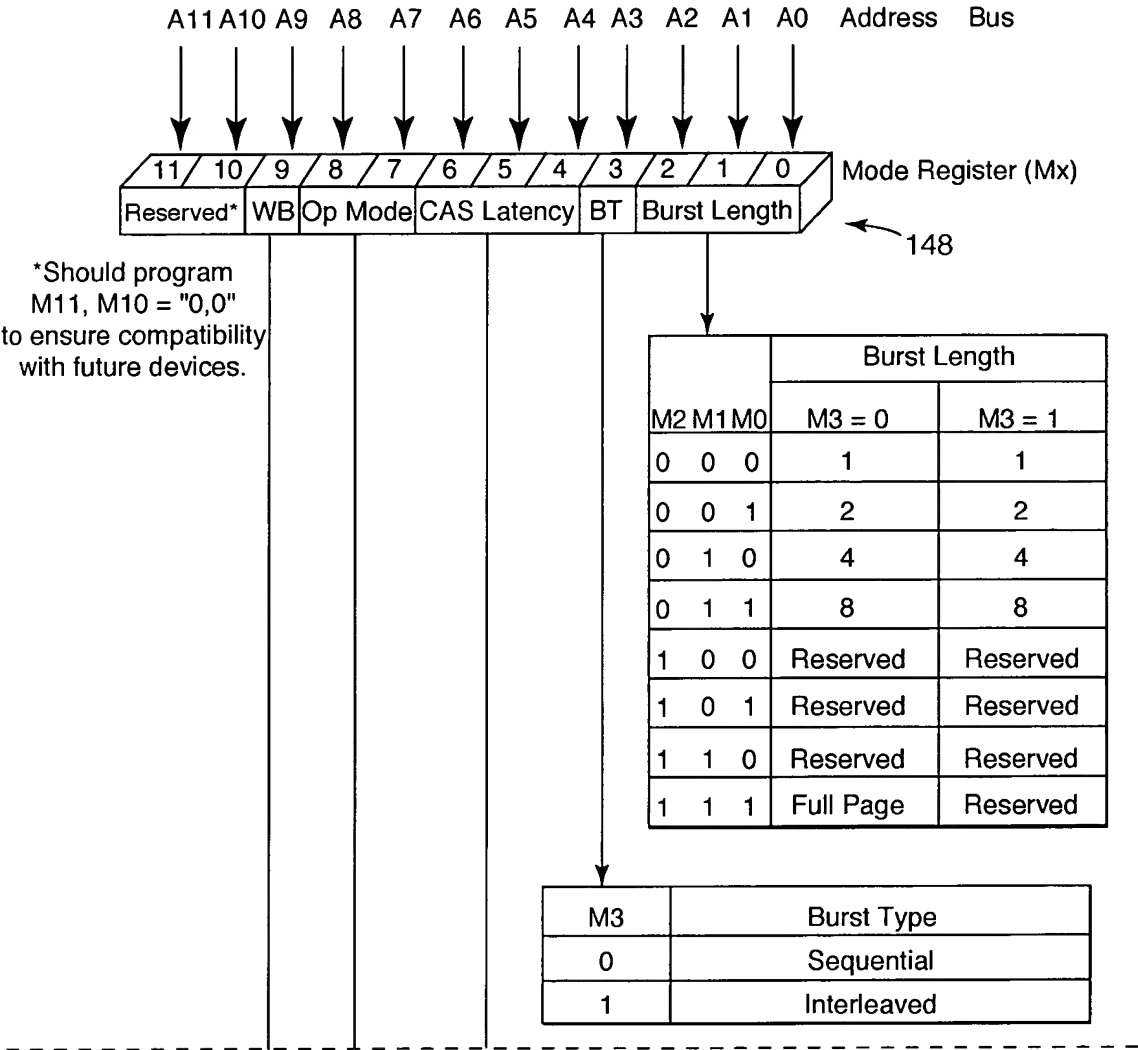


FIG. 2A

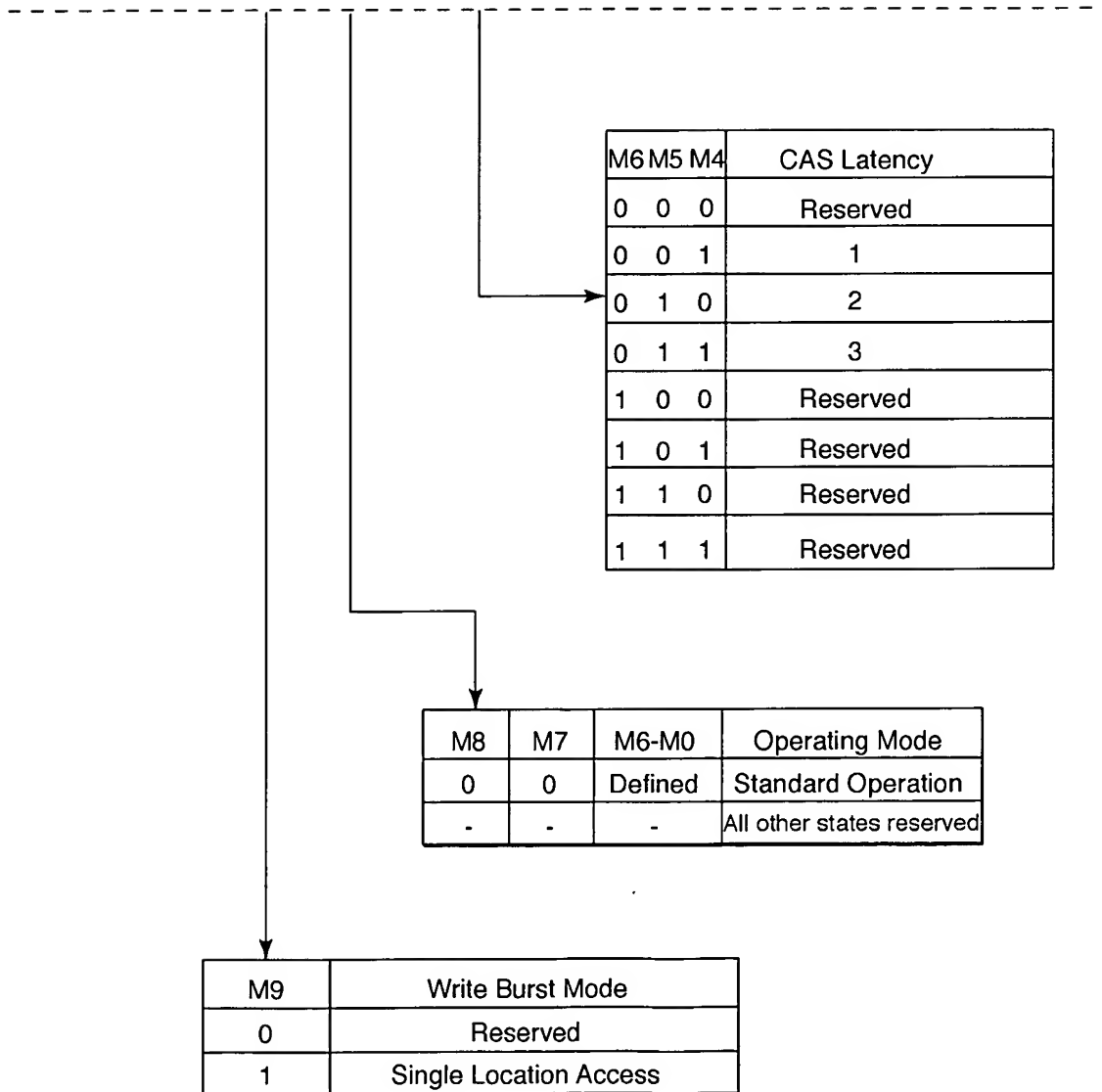


FIG. 2B

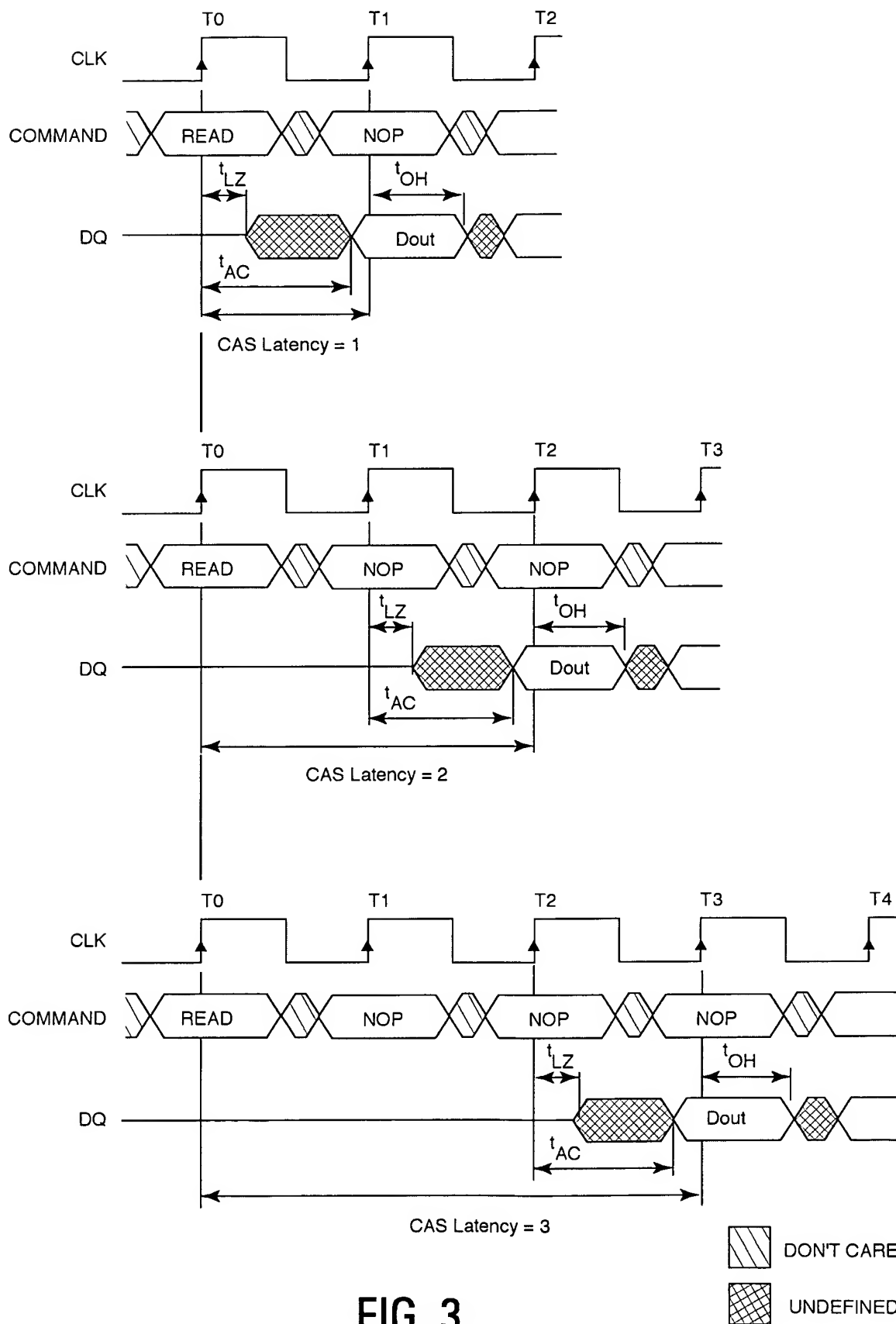
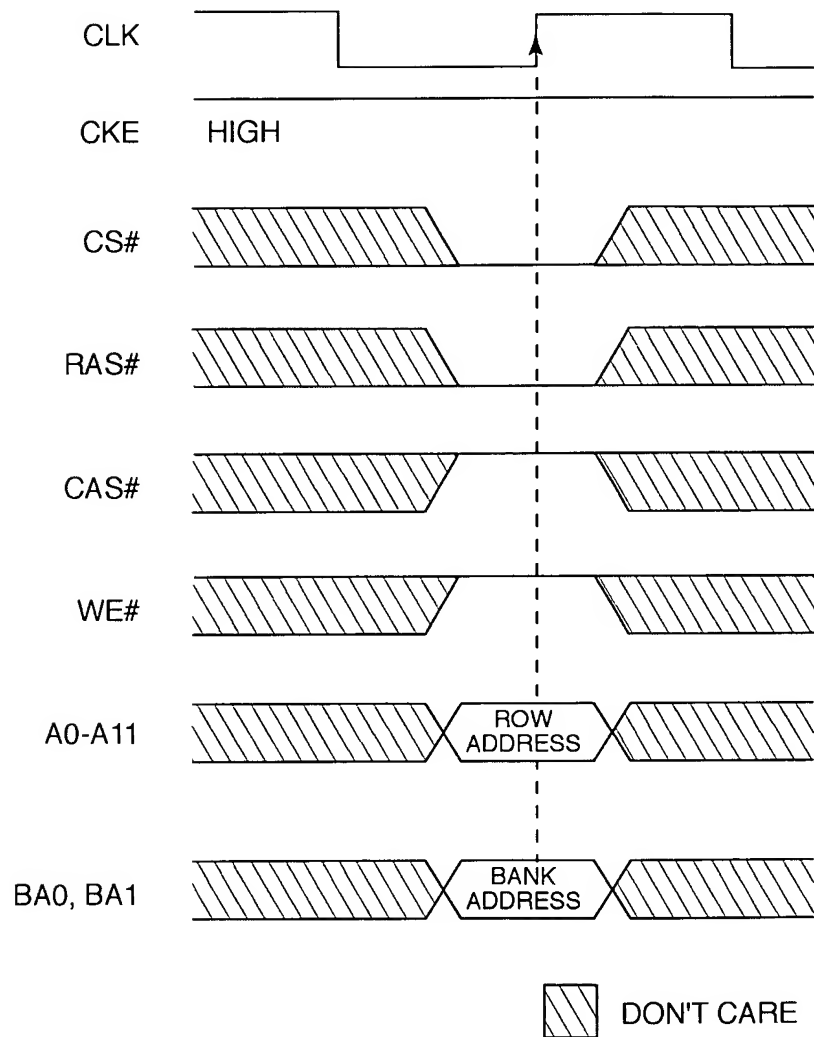


FIG. 3

**FIG. 4**

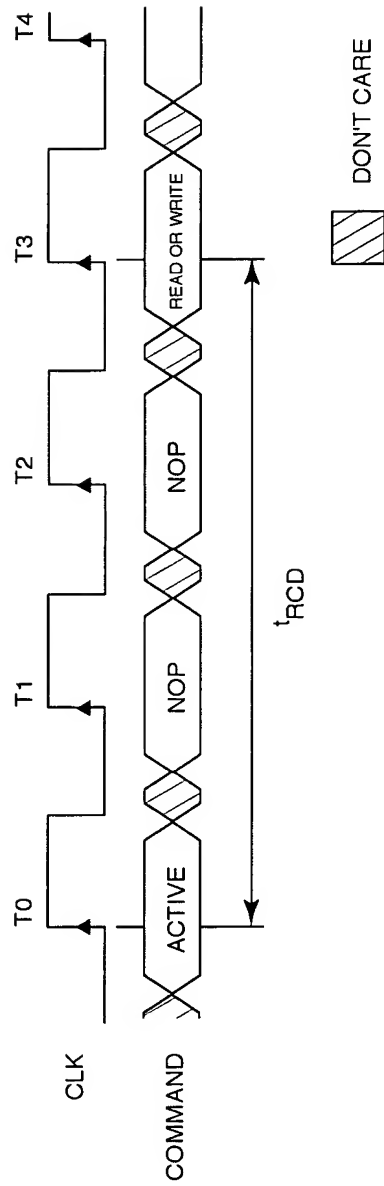
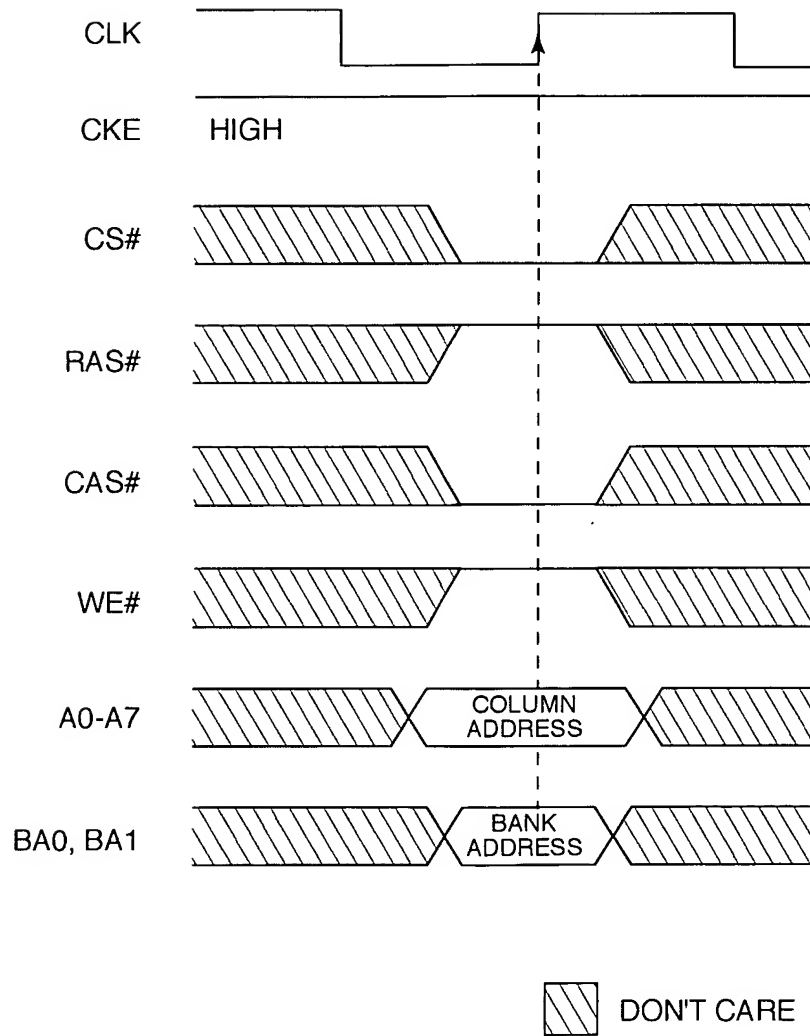
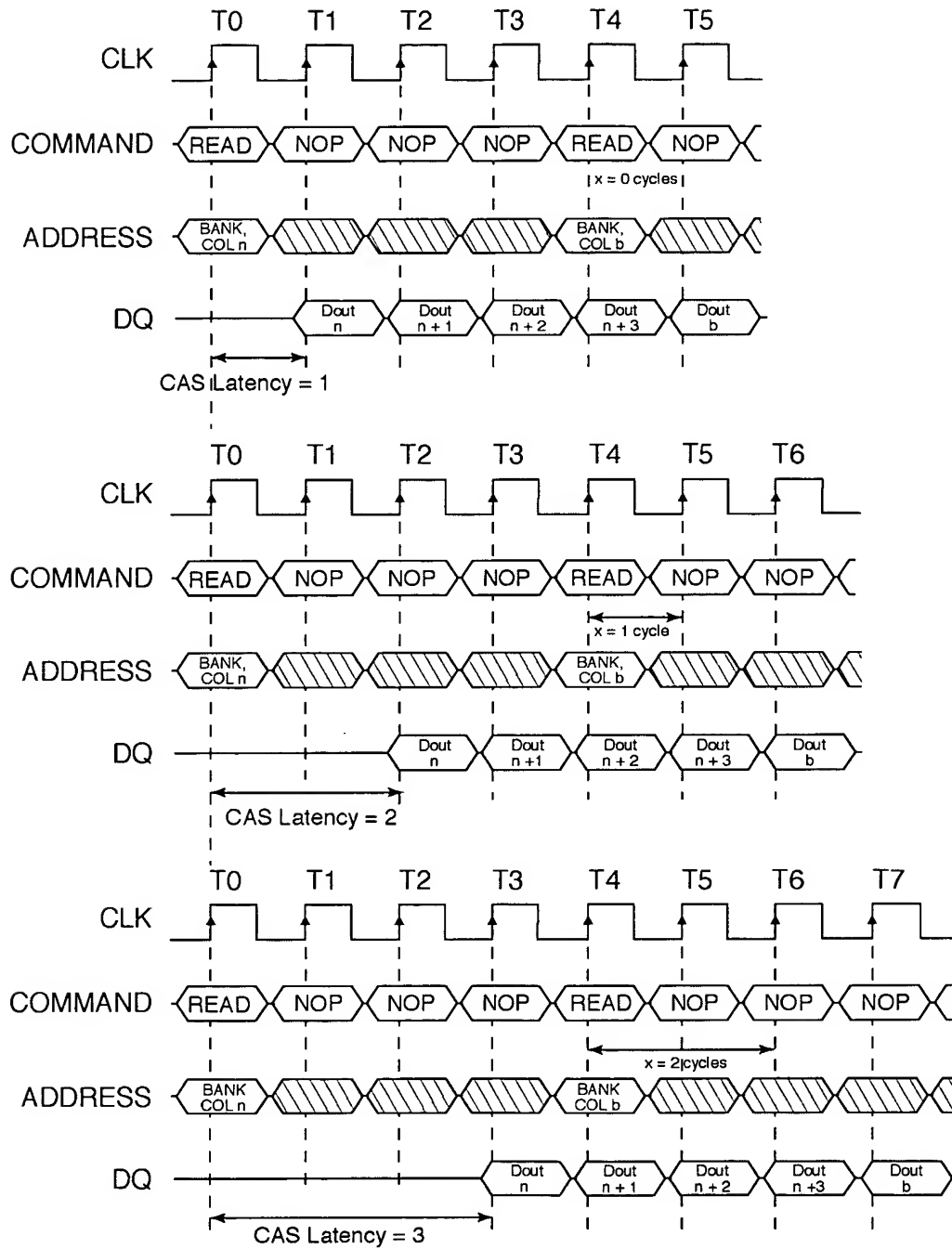


FIG. 5

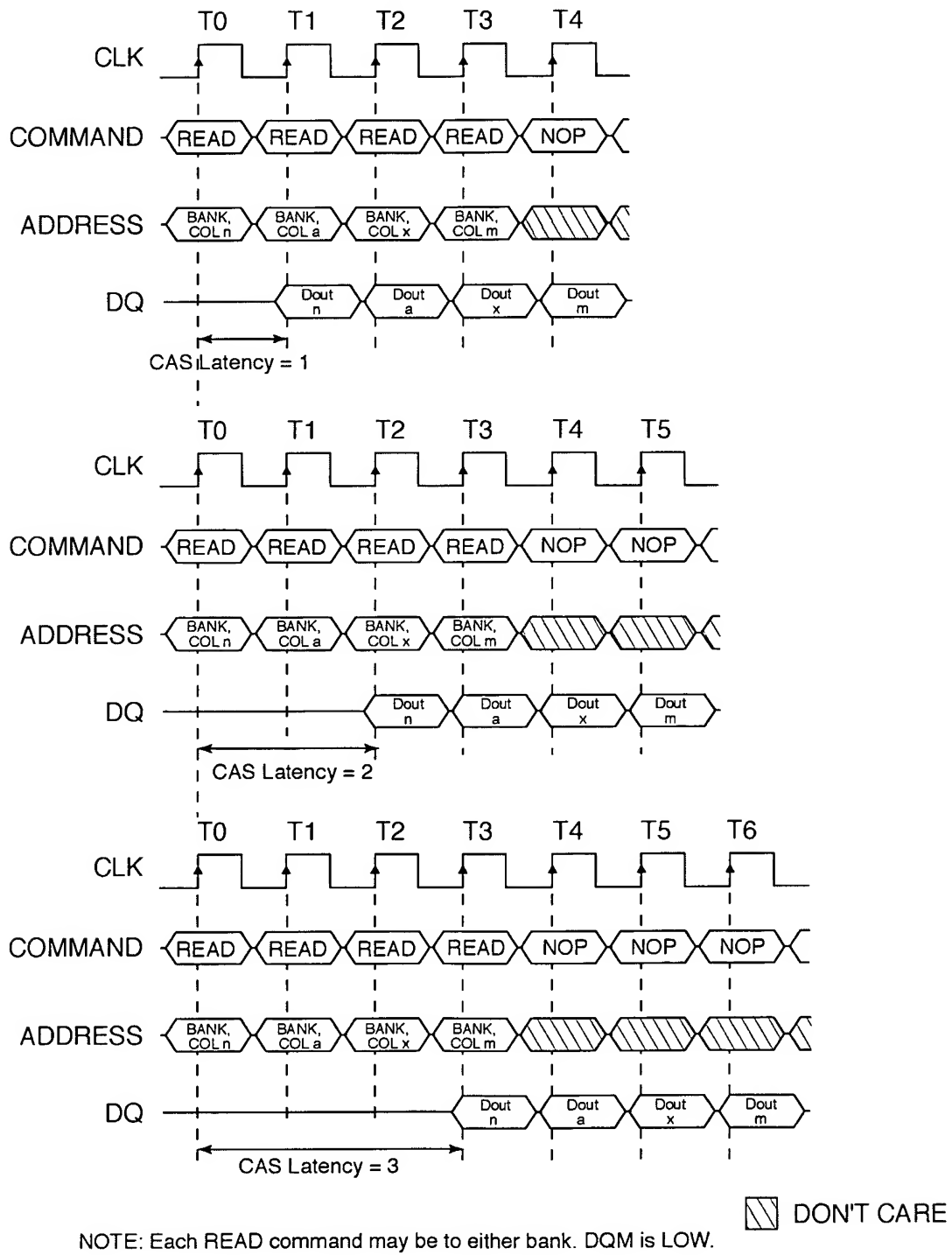
**FIG. 6**

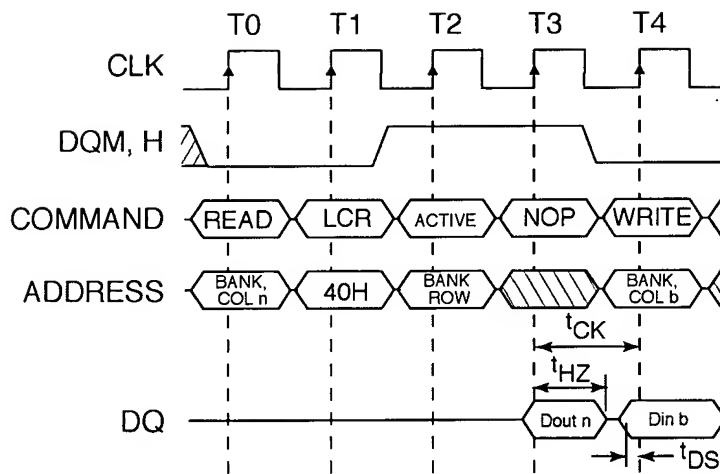


 **DON'T CARE**

NOTE: Each READ command may be to either bank. DQM is LOW.

FIG. 7

**FIG. 8**



NOTE: A CAS latency of three is used for illustration. The READ command may be to any bank, and the WRITE command may be to any bank. If a CAS latency of one is used, then DQM is not required.

 DON'T CARE

FIG. 9

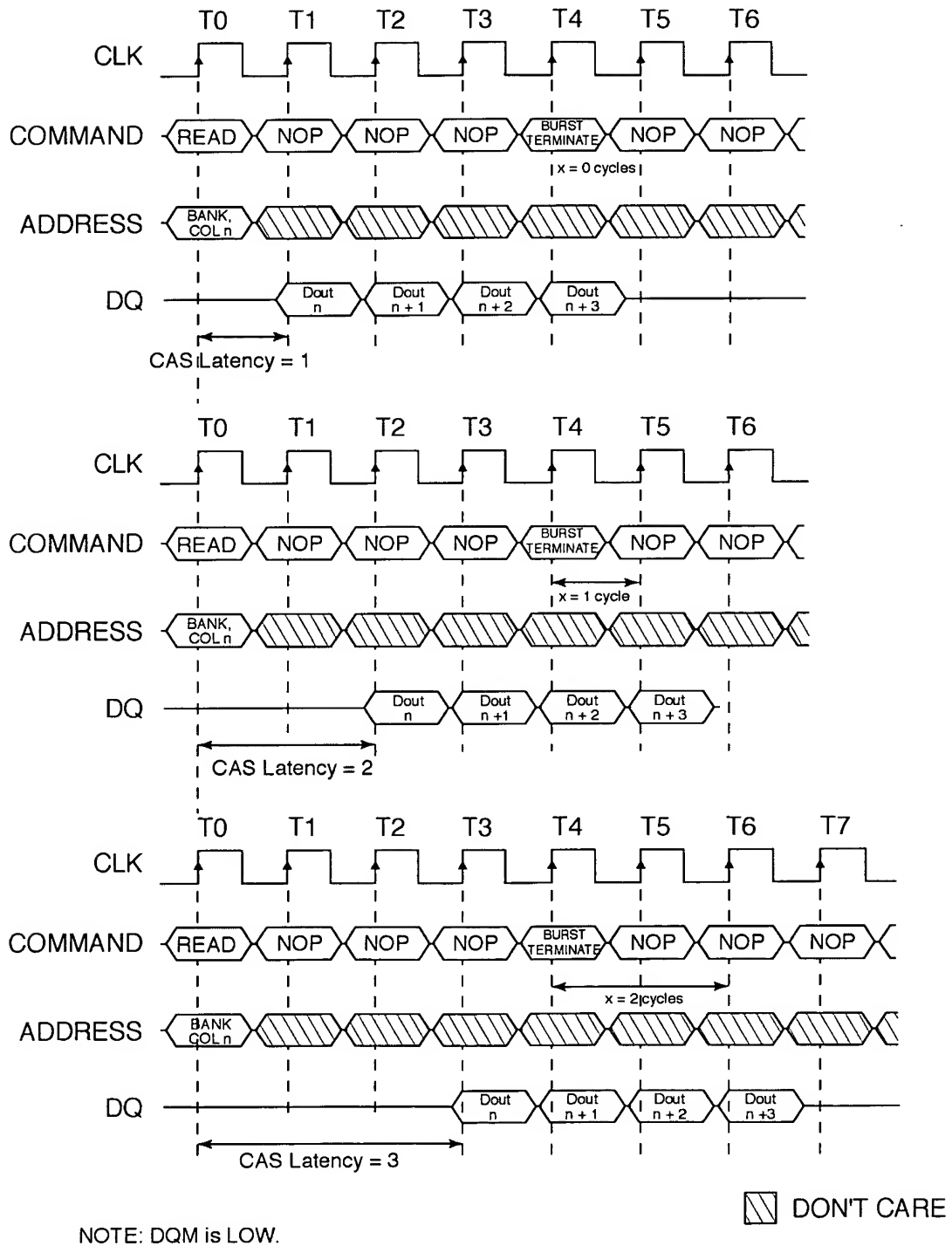


FIG. 10

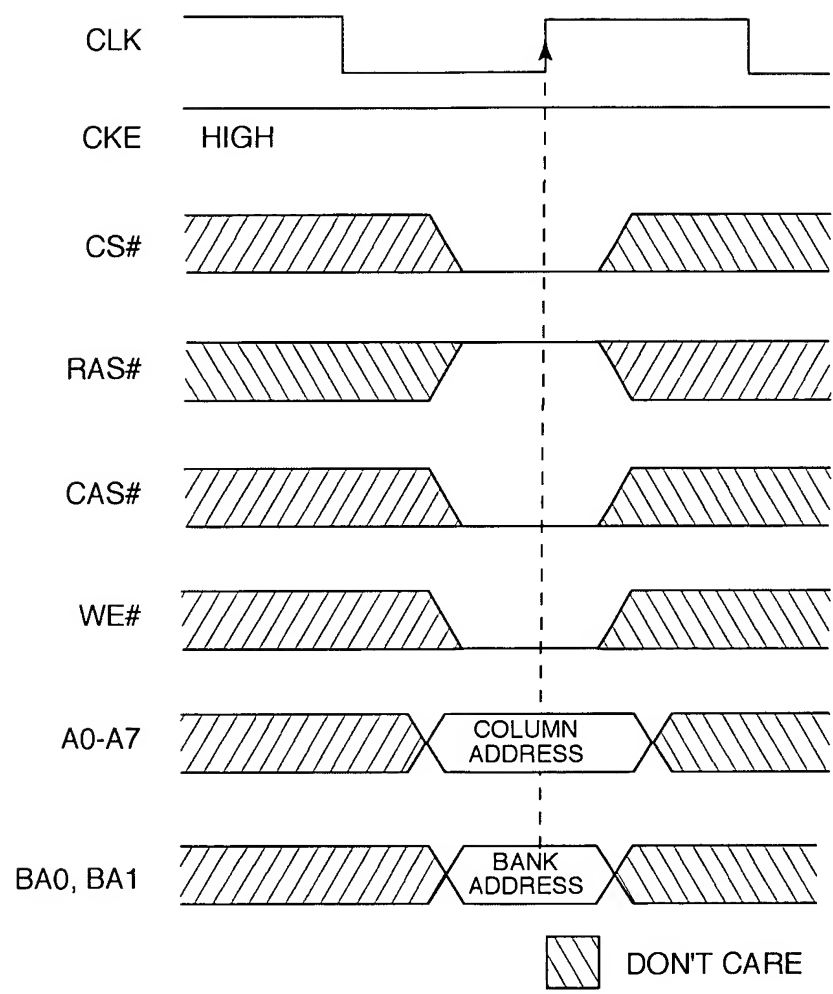
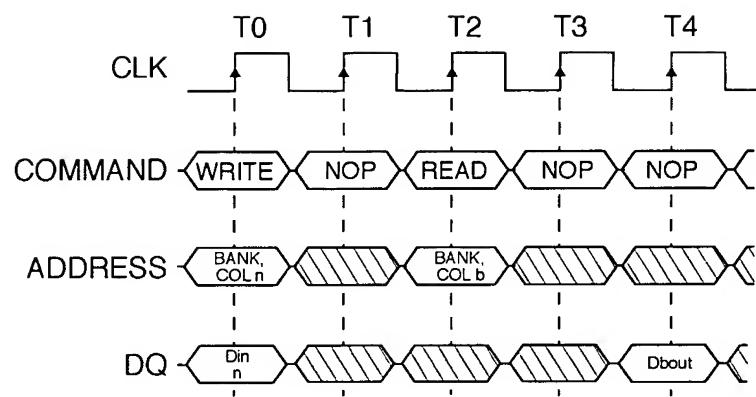


FIG. 11



NOTE: A CAS latency of two is used for illustration. The WRITE command may be to any bank and the READ command may be to any bank. DQM is LOW. A READ to the bank undergoing the WRITE ISM operation may output invalid data.

 DON'T CARE

FIG. 12

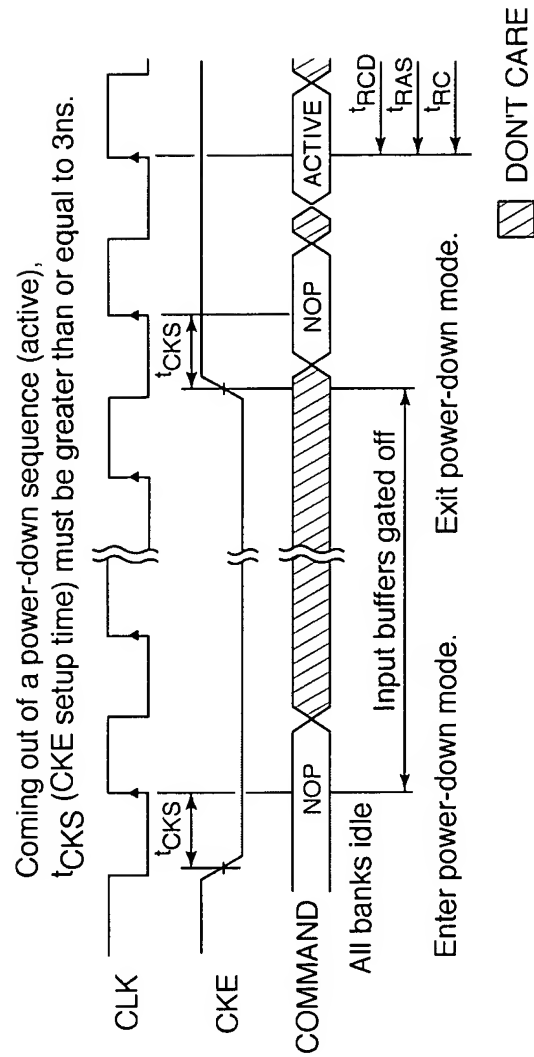


FIG. 13

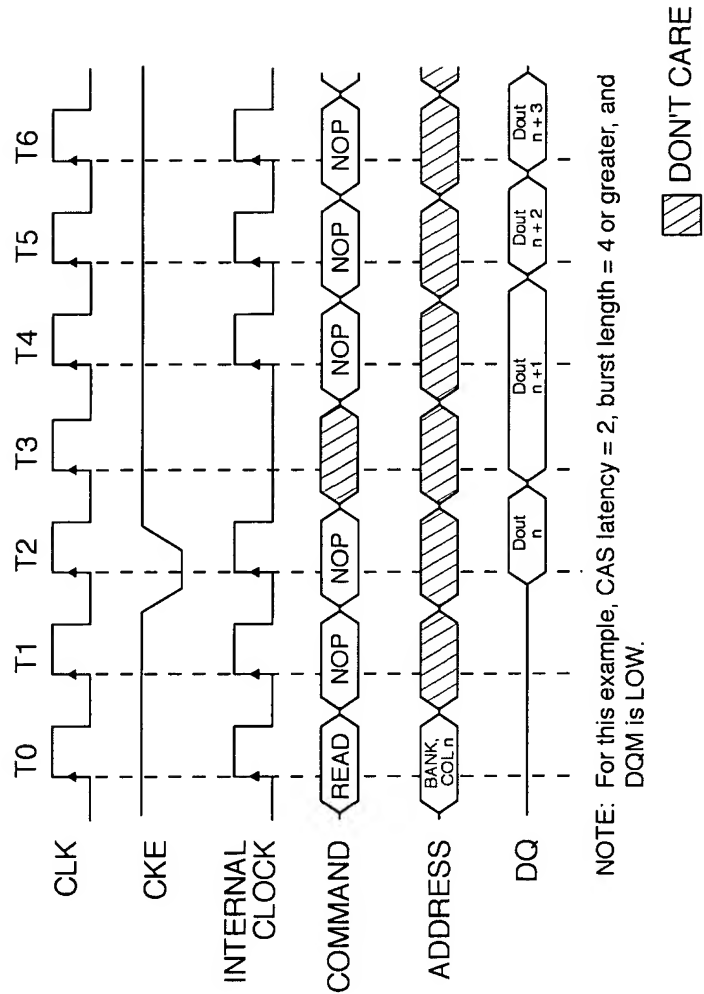




FIG. 14

ADDRESS RANGE

	Bank	Row	Column		
Bank 3	3	FFF	FFH	256K-Word Block	15
	3	C00	00H		
	3	BFF	FFH	256K-Word Block	14
	3	800	00H		
	3	7FF	FFH	256K-Word Block	13
	3	400	00H		
	3	3FF	FFH	256K-Word Block	12
	3	000	00H		
Bank 2	2	FFF	FFH	256K-Word Block	11
	2	C00	00H		
	2	BFF	FFH	256K-Word Block	10
	2	800	00H		
	2	7FF	FFH	256K-Word Block	9
	2	400	00H		
	2	3FF	FFH	256K-Word Block	8
	2	000	00H		
Bank 1	1	FFF	FFH	256K-Word Block	7
	1	C00	00H		
	1	BFF	FFH	256K-Word Block	6
	1	800	00H		
	1	7FF	FFH	256K-Word Block	5
	1	400	00H		
	1	3FF	FFH	256K-Word Block	4
	1	000	00H		
Bank 0	0	FFF	FFH	256K-Word Block	3
	0	C00	00H		
	0	BFF	FFH	256K-Word Block	2
	0	800	00H		
	0	7FF	FFH	256K-Word Block	1
	0	400	00H		
	0	3FF	FFH	256K-Word Block	0
	0	000	00H		

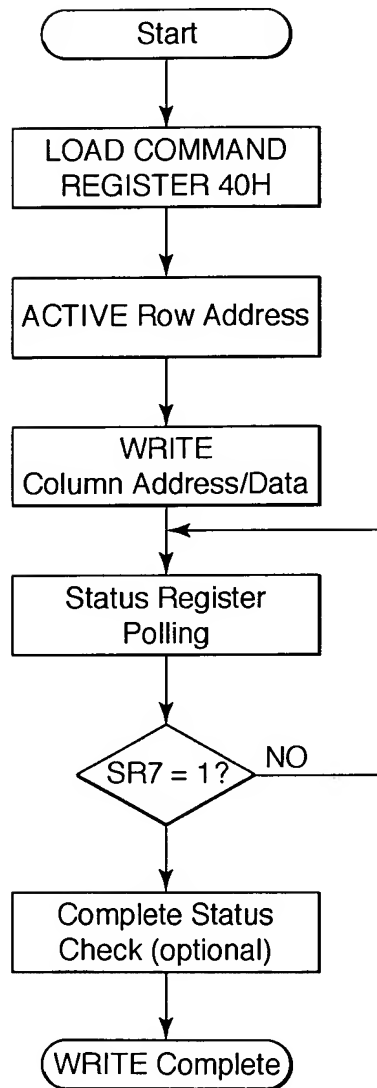
Word-wide (x16)

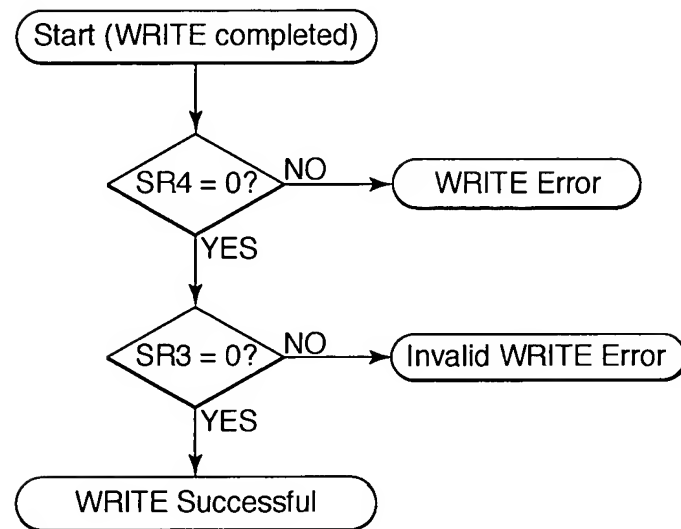
 Software Lock = Hardware-Lock Sectors
RP# = V_{HH} to unprotect if either the
block protect or device protect bit is set.

 Software Lock = Hardware-Lock Sectors
RP# = V_{CC} to unprotect but must be V_{HH}
if the device protect bit is set.

See BLOCK PROTECT/UNPROTECT SEQUENCE for
detailed information.

FIG. 15

**FIG. 16**

**FIG. 17**

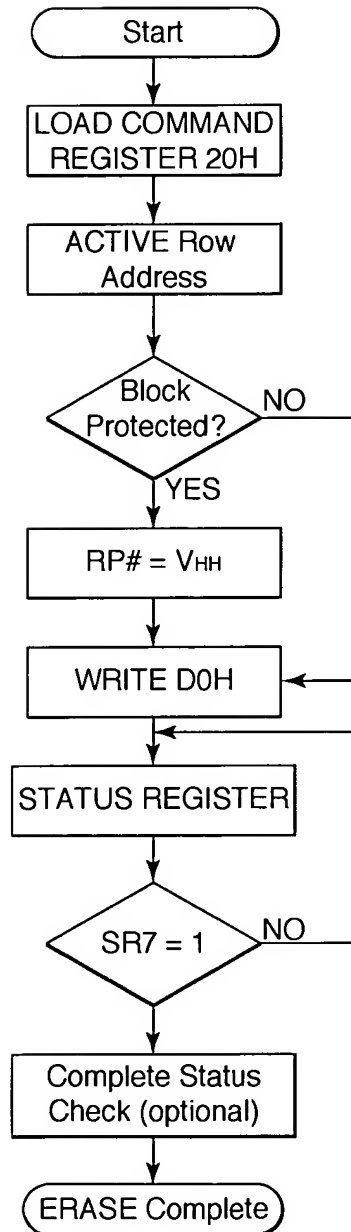
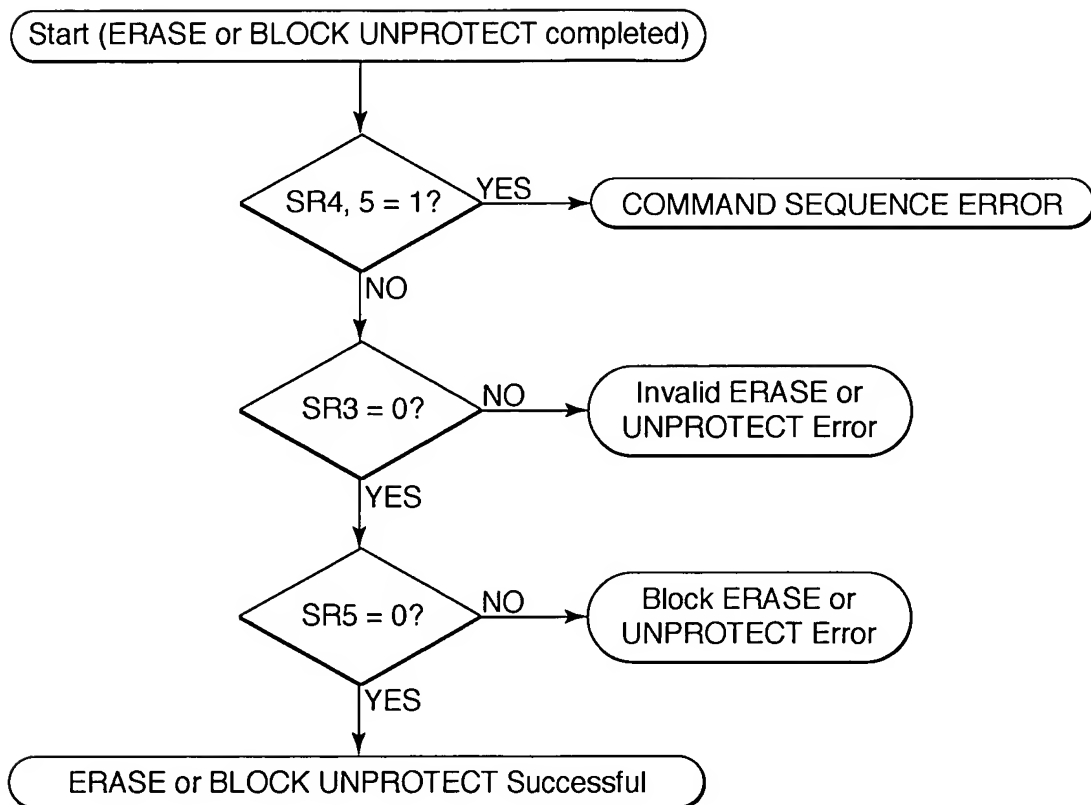


FIG. 18

**FIG. 19**

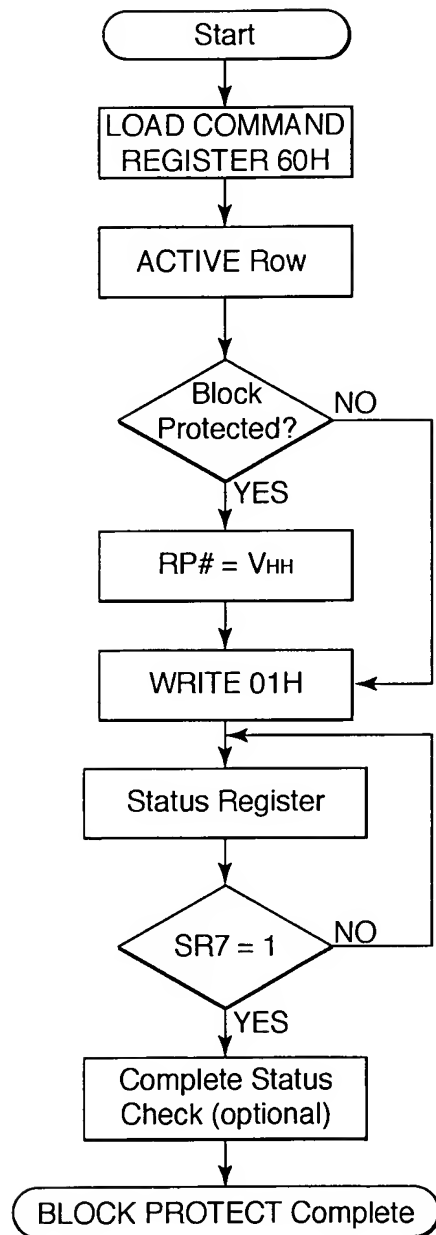
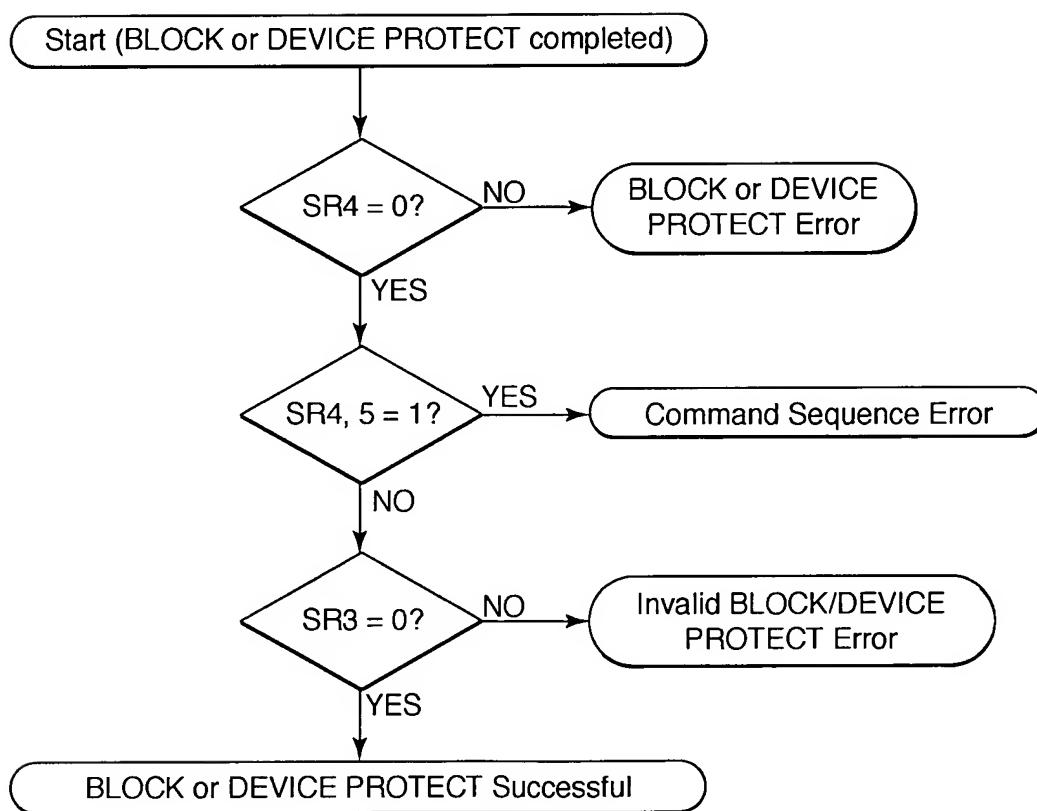
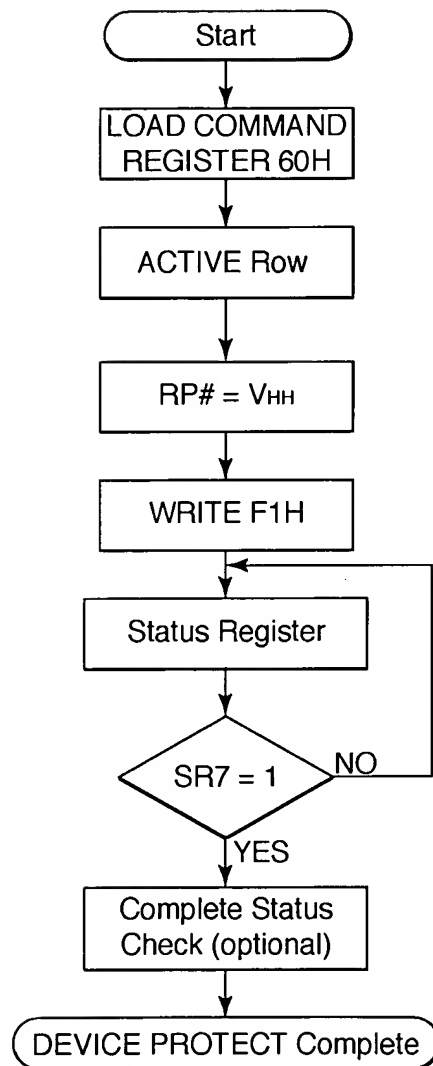
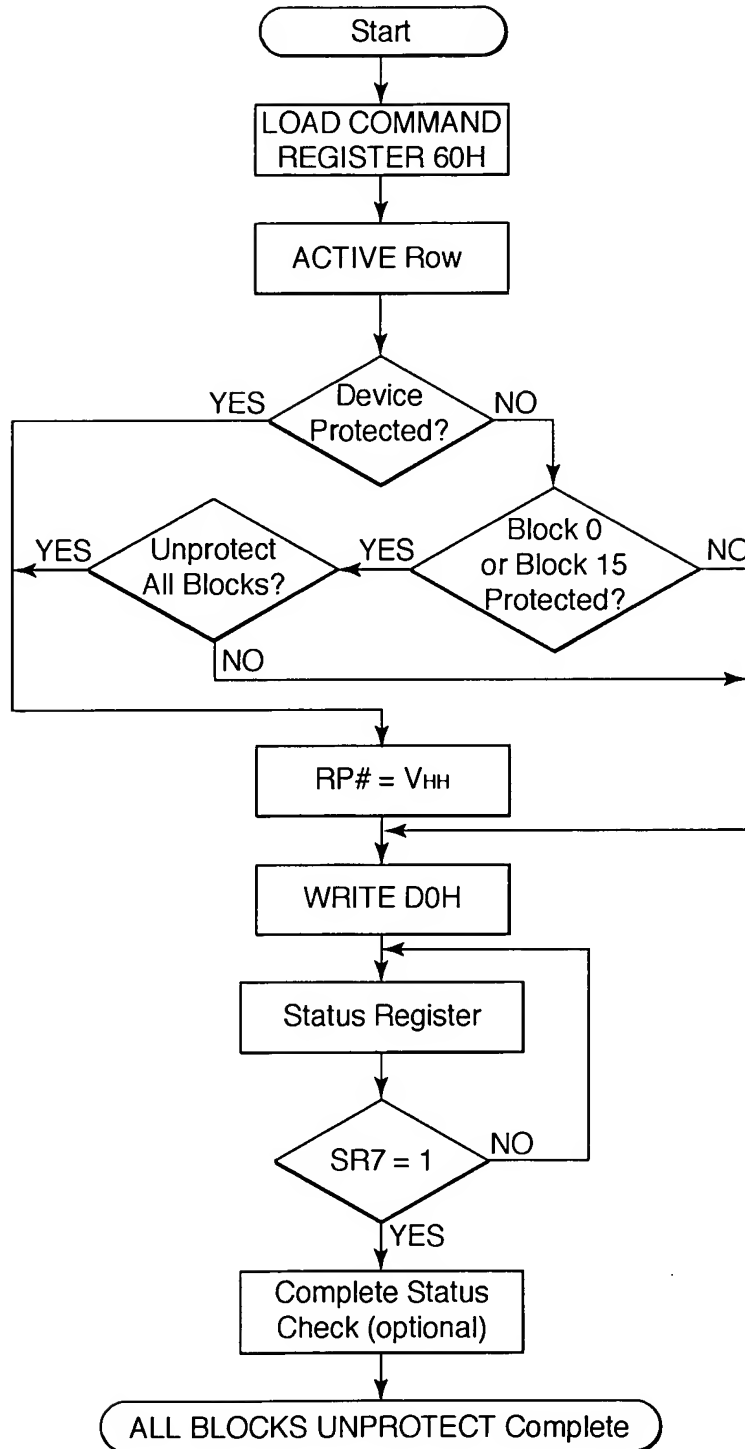


FIG. 20

**FIG. 21**

**FIG. 22**

**FIG. 23**

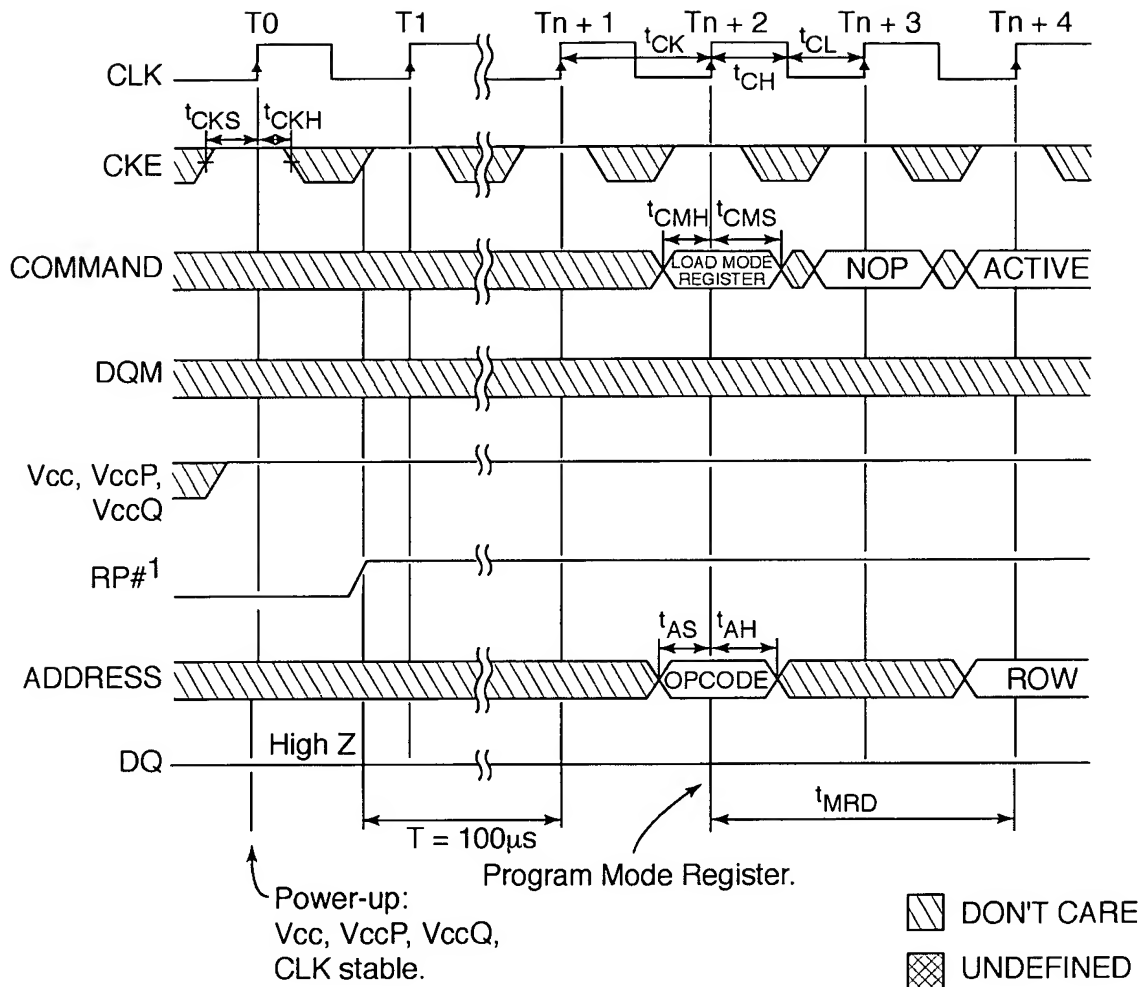


FIG. 24

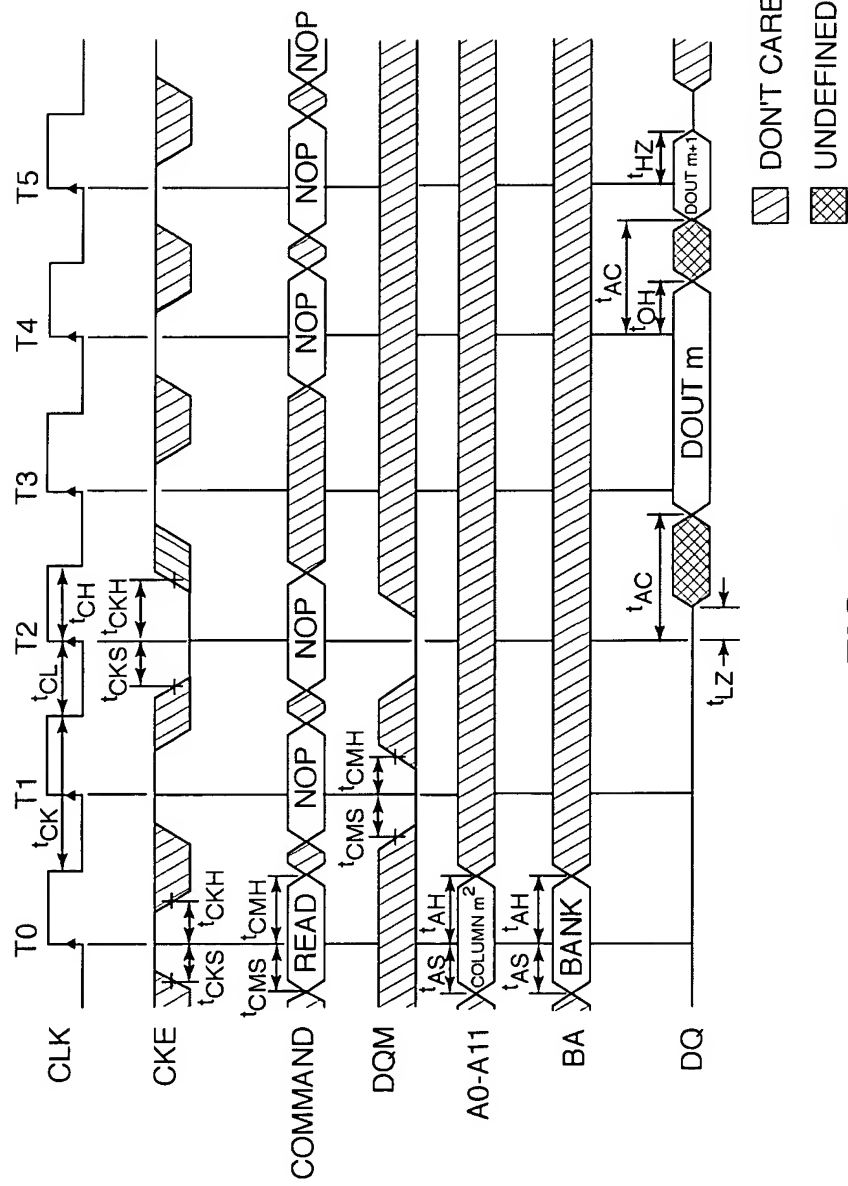


FIG. 25

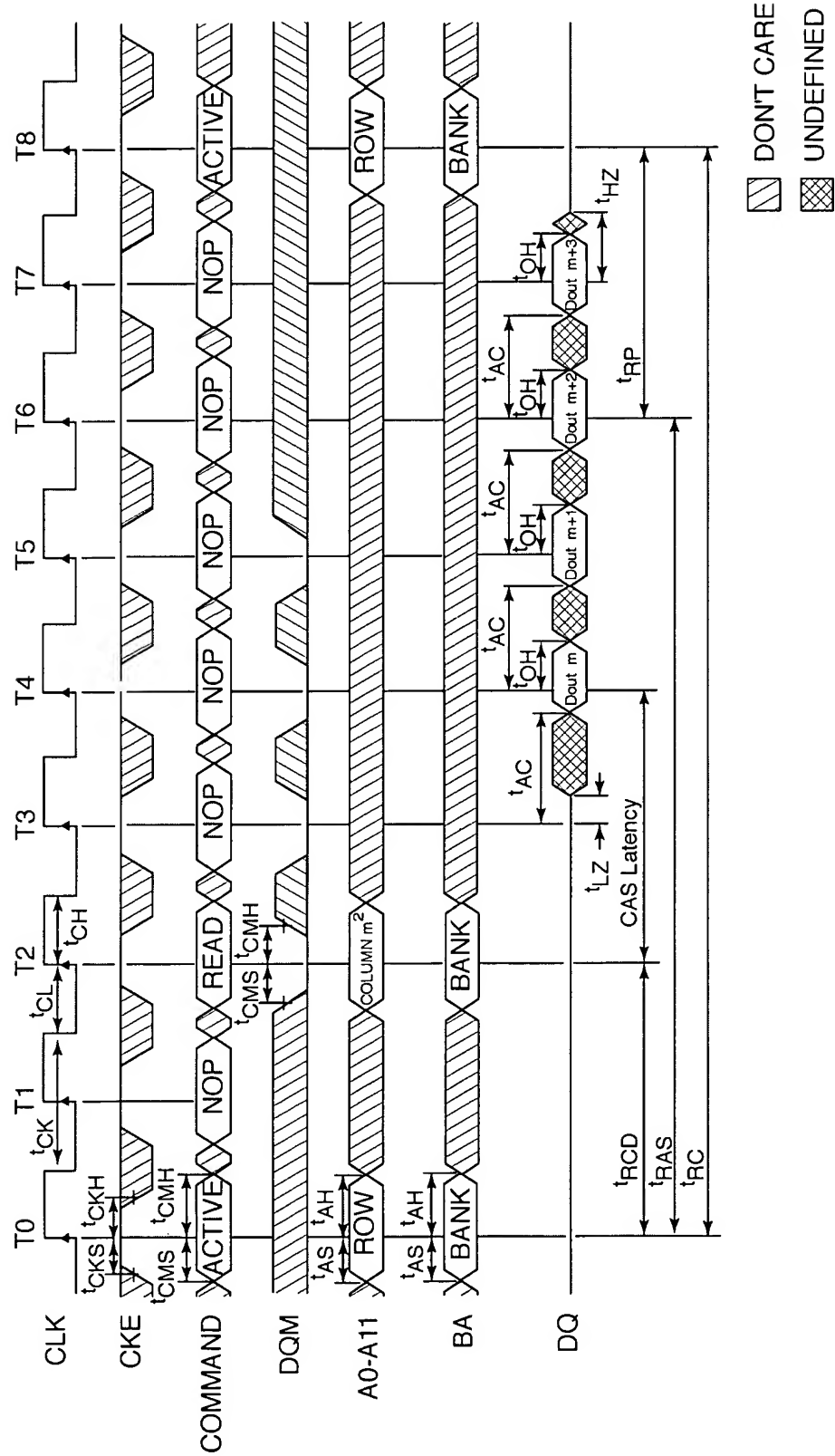


FIG. 26

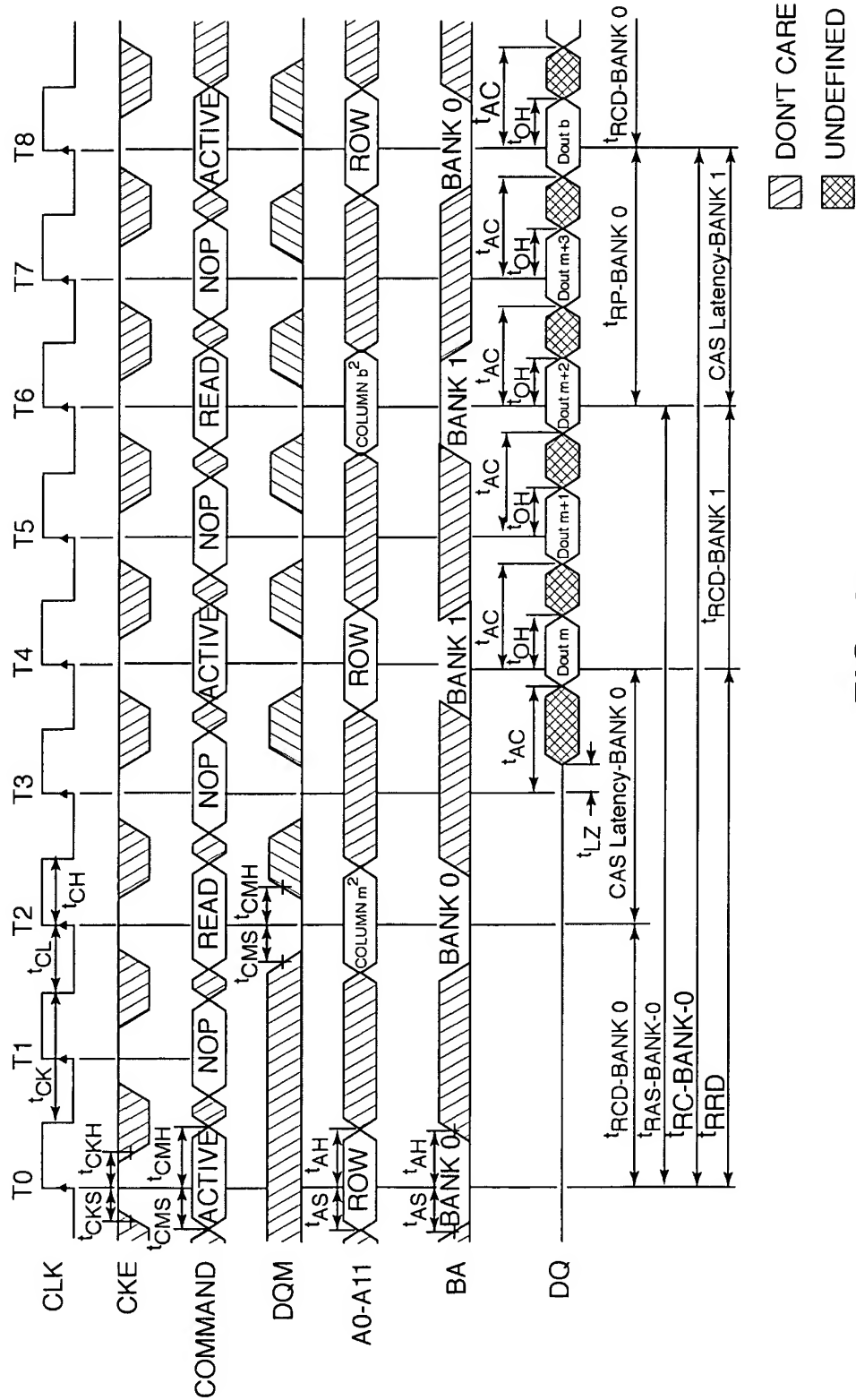


FIG. 27

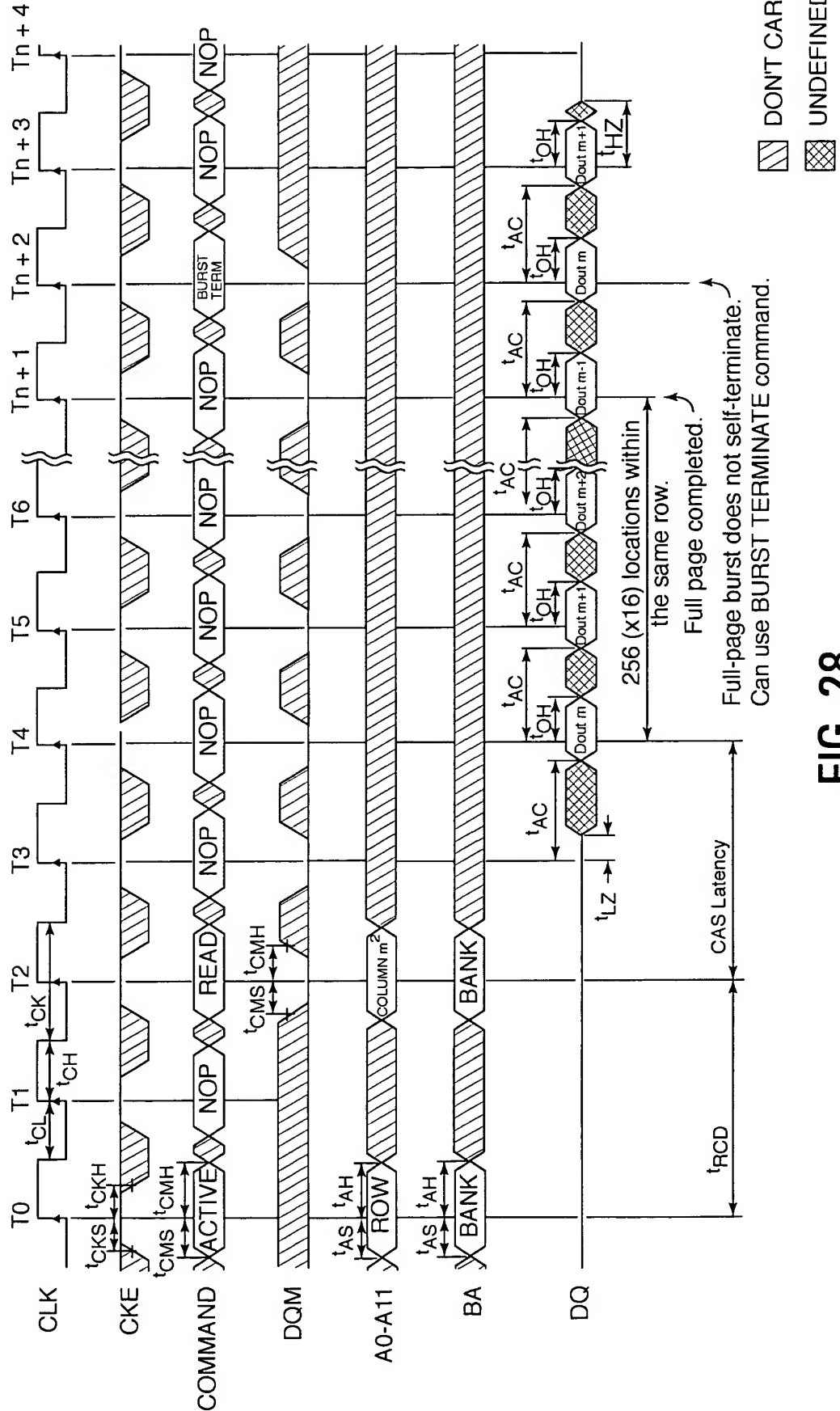


FIG. 28

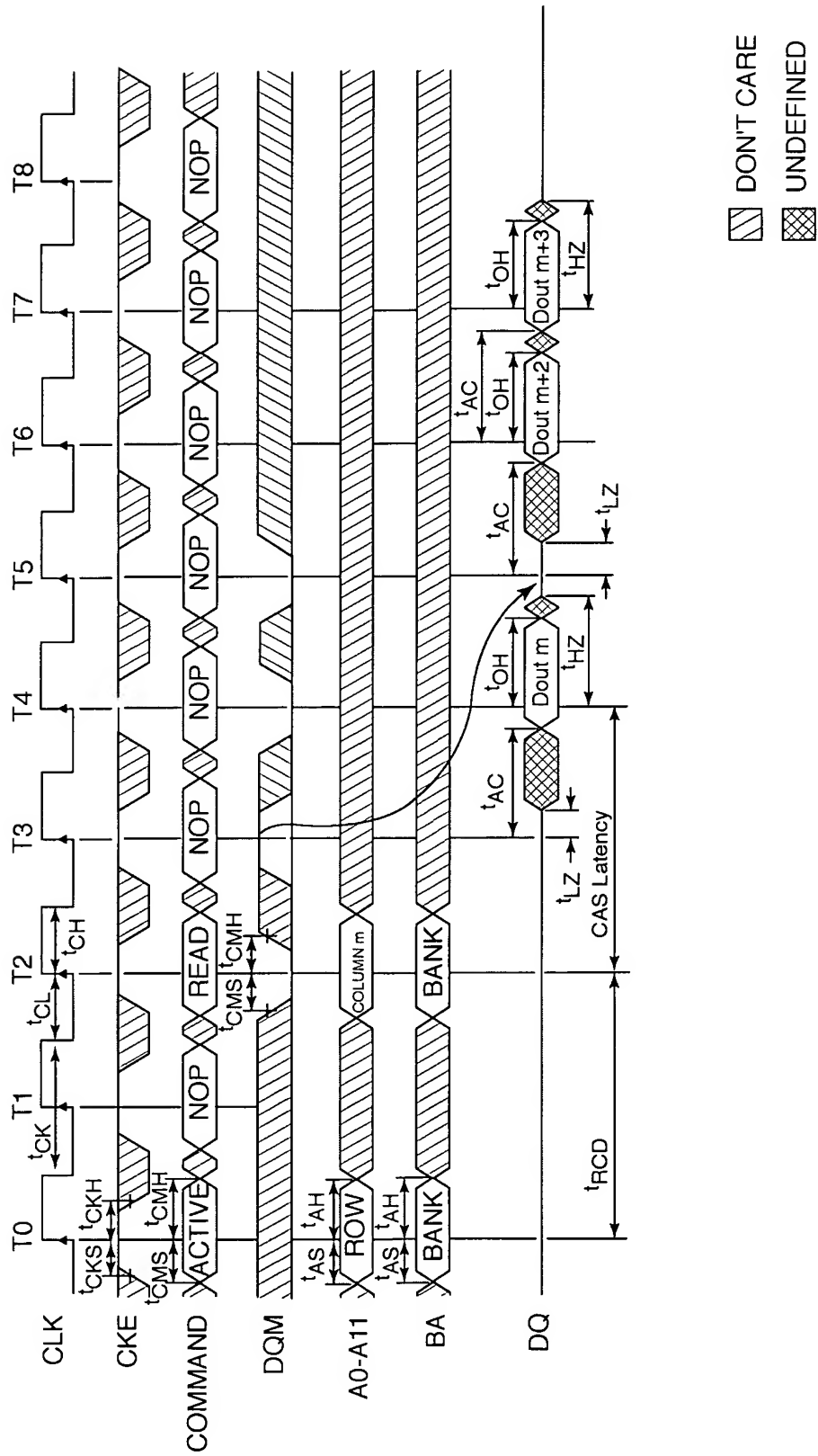


FIG. 29

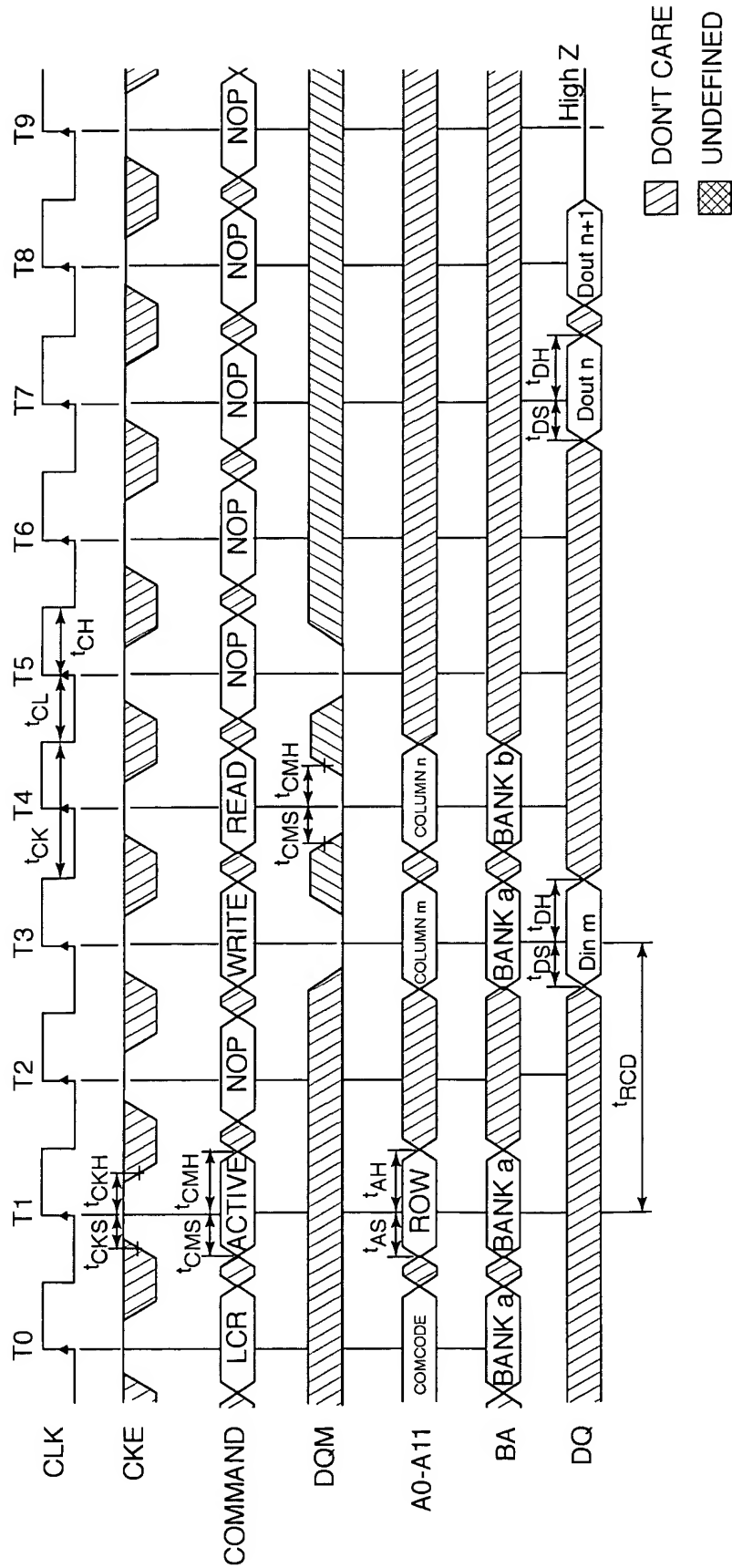


FIG. 30

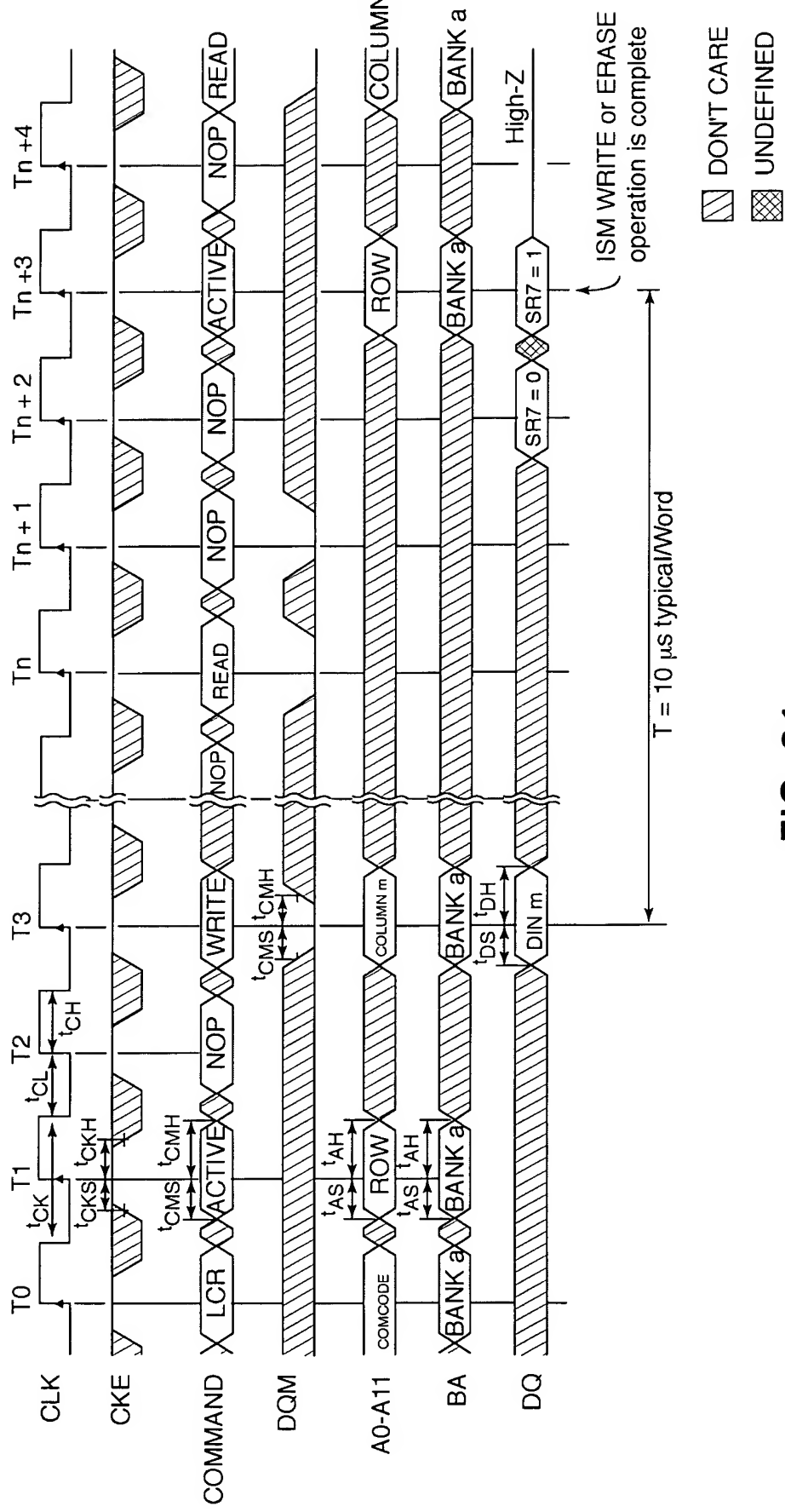


FIG. 31

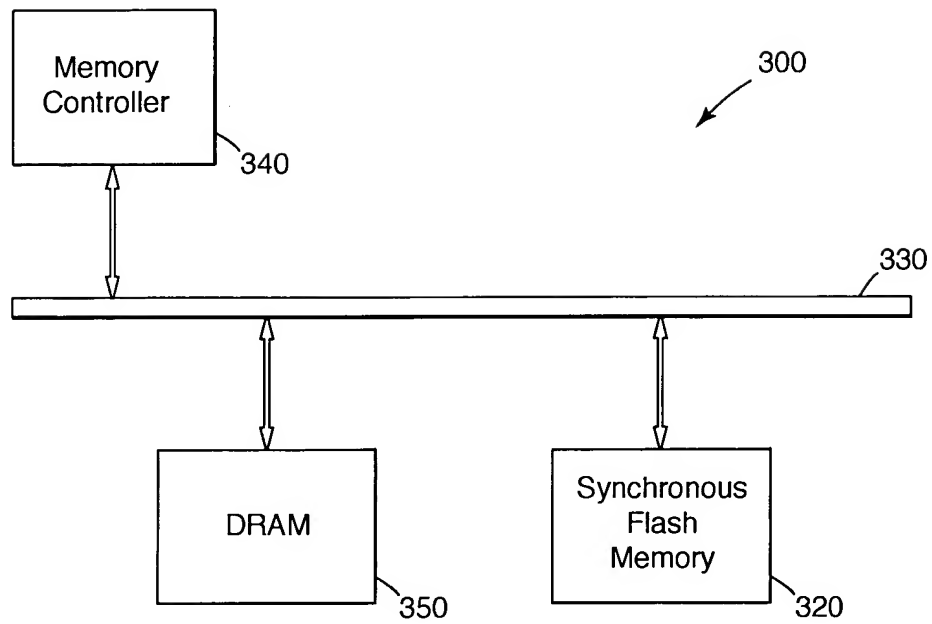


FIG. 32